IN THE SPECIFICATION:

Please replace the paragraph beginning at line 15 on page 42 with the following paragraph.

The memory of the Cache 615 is preferably a Dual-Port RAM, used as a cache between the PDSP 114 and SDRAM (located off chip) or other similar remote memory device, the SDRAM is accessible through the chip/peripheral interface. The cache 615 can be logically partitioned into a plurality of queue each queue containing N cells (RAM sized based on the application). The SDRAM (located off chip) or other similar remote memory device can be configured to include a dedicated queue corresponding to each of the plurality of queues in the Cache 615.

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